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Cascaded 61-level Envelope Type Asymmetric Multilevel Inverter with Binary configuration

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Abstract
This paper presents single phase 61 level E- Type MLI performance. A new E-Type module for asymmetrical MLI's with reduced components, each of the module produces 13 levels with four unequal DC sources and 10 switches. The design of the proposed module makes some preferable features with a better quality than similar modules such as the low number of semiconductors and DC sources and low switching frequency. Also, this module is able to create a negative level without any additional circuit such as an H-bridge which causes reduction of voltage stress on switches. Cascade connection of the proposed structure leads to a modular topology with more levels and higher voltages. The control techniques play a very important role in reducing total harmonic distortion hence a review on different control technique presented Half height method and Equal phase control technique scheme is used to achieve high quality output voltage with lower harmonics. MATLAB simulations and practical results are presented to validate the proposed module good performance. Module output voltage satisfies harmonics standard without any filter in output.

Keywords: Asymmetric components, E-Type, Multilevel inverter, Power electronics, Half Height method, Equal phase method

1. Introduction
Multilevel inverters (MLIs) have been innovated as necessary cost benefit devices with a wide range of applications. Multilevel inverters generate an AC voltage using small voltage steps obtained with the help of DC supplies or capacitor bank. Output voltage obtained from multilevel inverters are superior in quality and need less or no filter requirements there by reducing the overall system size. The output voltage of the multilevel inverter gets improved by increasing its number of levels. It also reduces the total harmonic distortion (THD) on the output hence improving the power quality of the overall system. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy source such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter for a high-power application. Multilevel converters are different arrangements of semiconductor switches with DC links to create n- level output waveform. This paper presented different tried to reach more levels with lower components. Asymmetric multilevel inverters which have unequal DC links become interesting in order to increase the quality of output waveform by minimizing the number of components. This paper aims to achieve maximum capacity from DC link by a suitable arrangement of switches which improves economic implementation cost, switching frequency, TSV, number of levels, and THD. It presents a new asymmetric multilevel module based on cascade category which does not need any additional circuit to create negative voltage levels. Also, it makes 13 levels by reduced switches. Section 2 illustrates proposed multilevel inverters including module description, switching patterns, cascade connection and comparison table with similar modules. Half height method and Equal phase control technique is introduced for switching modulation in section 2. Simulation and experimental results are shown in sections 3, and 4, respectively. Conclusions are presented in section 5.

2. Proposed envelope type inverter
A new topology of asymmetric multilevel modular with a new component arrangement including 10 switches, 10 diodes and 4 unequal DC sources (two 2, two 1VDC) named as Envelope type (E-Type). This arrangement synthesizes voltage sources produces 13 levels (6 positive level, 6 negative level and zero level) without any additional circuit. The main concept of this circuit is to create different paths from different sides of a DC source to be connected to other sources. Fig shows the

configuration of E-Type asymmetrical module in where DC sources are located in the middle of the circuit and are connected together to form different voltage levels via surrounding switch (S1-S6). A bidirectional switch (S7) is required to avoid short circuit of DC sources on left or right sides of the module. Another bidirectional switch (S8) is also needed to achieve voltage levels of ±5.

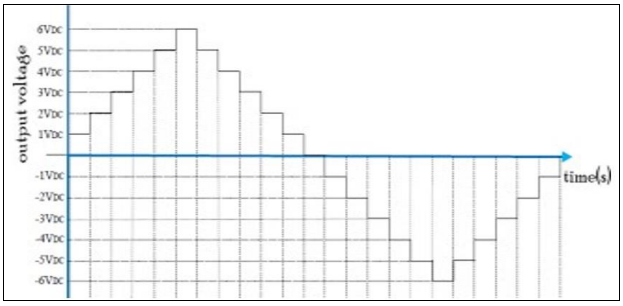


Fig 1: Waveform

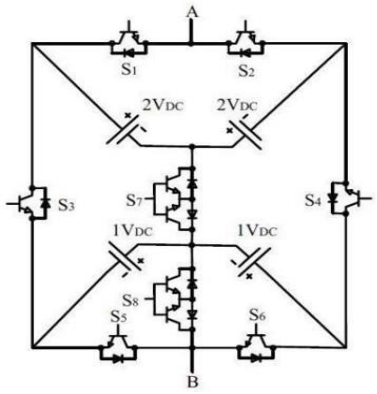


Fig 2: Envelope Type MLI

Table 1: Switching table

	S1	S2	S3	S4	S5	S6	S7	S8
1Vdc	1	0	0	0	0	1	1	0
2Vdc	1	0	0	0	0	0	1	1
3Vdc	1	0	0	0	1	0	1	0
4Vdc	1	0	0	1	0	1	0	0
5Vdc	1	0	0	1	0	0	0	1
6Vdc	1	0	0	1	1	0	0	0
-1Vdc	0	1	0	0	1	0	1	0
-2Vdc	0	1	0	0	0	0	1	1
-3Vdc	0	1	0	0	0	1	1	0
-4Vdc	0	1	1	0	1	0	0	0
-5Vdc	0	1	1	0	0	0	0	1
-6Vdc	0	1	1	0	0	1	0	0

Table Switching angle table

Modes of Operation

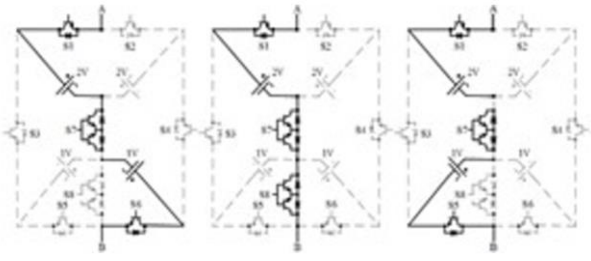


Fig 3: a) level +1, **b)** level +2, **c)** level +3

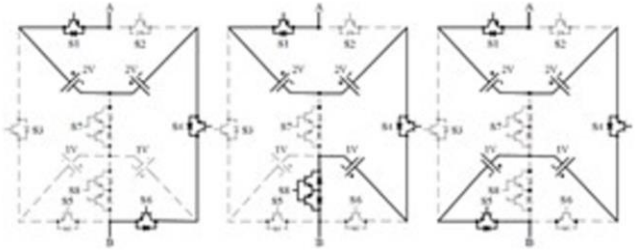


Fig 3: d) level +4, **e)** level +5, **f)** level +6

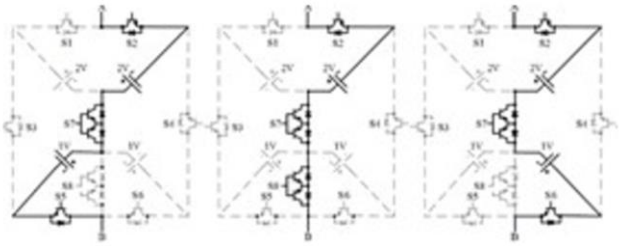


Fig 4: a) level -1, **b)** level -2, **c)** level -3

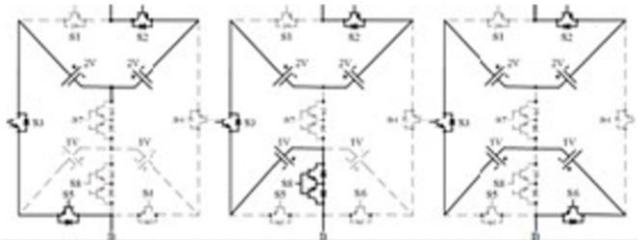


Fig 4: e) level -4, **f)** level -5, **g)** level -6

Section 1
Module Extension

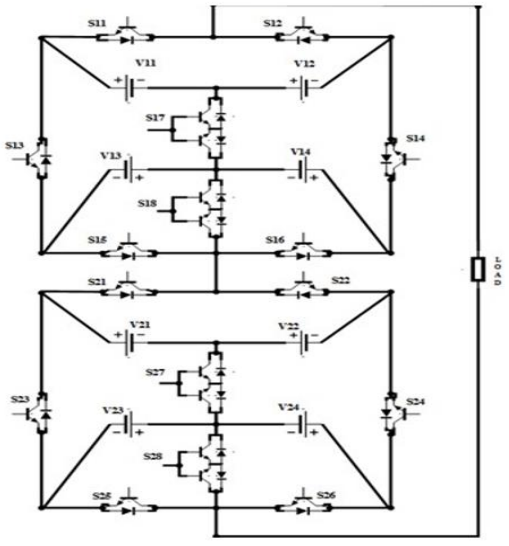


Fig 5: The Cascade Arrangement of Modular Proposed Multilevel Inverter

The circuit diagram of proposed 61 level Multilevel inverter as shown in figure. The two Envelope type modules are cascaded with binary configuration applied to DC sources to get desired 61 levels. Each envelope type modules consists of 8 switches with 2bidirectional and 4 voltage sources can able to generate 13 levels (6 positive, 6 negative and one zero). The proposed MLI circuit uses 16 switches with 4 bidirectional and 8 Asymmetrical voltage sources. The voltage sources can be renewable sources like PV

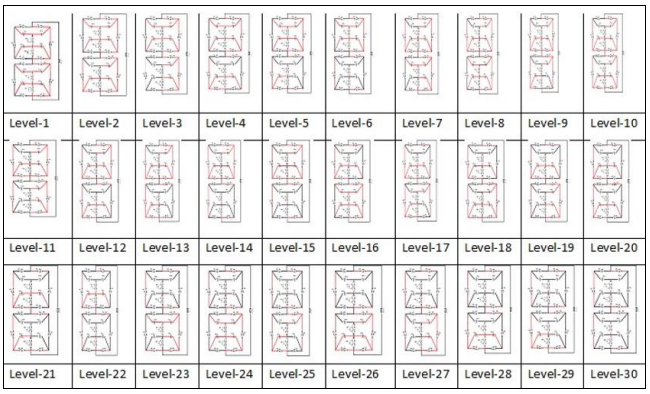
cells or energy storing elements like Batteries or capacitors. The voltage sources used is in Binary configuration 1:2:4:8. i.e., two 12VDC, two 24 VDC, two 48 VDC and two 96 VDC.

This circuit arrangement synthesis voltage sources to produce 61 output levels. (30 positive, 30 negative and one zero level) without any additional circuit to generate positive or negative voltage levels

In each of the two modules the DC sources are located in the middle of the circuit connected together to form different voltage levels via surrounding switches (S11 – S16) and (S21 –* S26). The bidirectional switches S17 and S27 are required to avoid short circuit of DC sources of left and right side of the modules. Another bidirectional switch pairs S18 and S28 are required to achieve the voltage levels of multiplies of ± 5 VDC.

Modes of Operation

Positive cycle



Negative Cycle

Expected Waveform

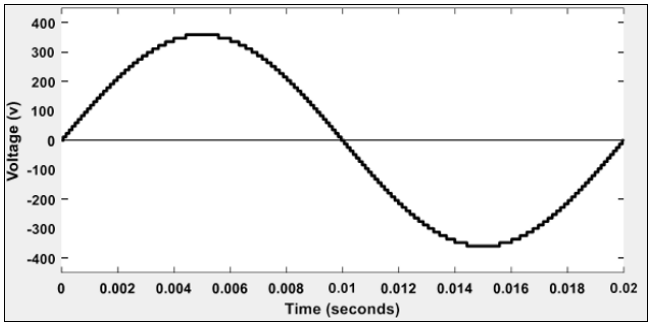


Fig 6: Expected Waveform For 61 level Multi Level Inverter

The design of the proposed 61 level Multilevel inverter

For an Asymmetrical configuration of Envelope type modules,

The total number of switches required for each modules is given by the equation

$$N = 8\ m\ldots$$

Where, N = number of switches m = number of modules

In the proposed Multilevel inverter, the number of modules is given by m = 2

Therefore, The total number of switches = 8 * m = 8 * 2 =16

The number of DC link voltage sources required for each modules is given by

$$K = 4\ m\ldots$$

Where, K = number of voltage sources m = number of modules

The total number of voltage sources = 4 * 2 = 8

For the proposed circuit voltage sources are designed with Binary configuration i.e., 1Vdc:2Vdc:4Vdc:8Vdc. The Vdc value selected for the proposed circuit is given by 12Vdc, hence all different voltage source values are given by

$V_{11} = V_{12} = 1$ Vdc = 1* 12 = 12V
$V_{13} = V_{14} = 2$ Vdc = 2 * 12 = 24V
$V_{21} = V_{22} = 4$ Vdc = 4 * 12 = 48V
$V_{23} = V_{24} = 8$ Vdc = 8 * 12 = 96V

The maximum voltage for the asymmetrical connection of the Envelope type modules and the RMS voltage s found using equation

$$V_{max} = V_{11} + V_{12} + V_{13} + V_{14} + V_{21} + V_{22} + V_{23} + V_{24}$$

$$V_{max} = 12+12+24+24+48+48+96+96 = 360\ V$$

$$V_{RMS} = \frac{Vmax}{\sqrt{2}}$$

$$V_{RMS} = 360/\sqrt{2} = 254.55\ V$$

The proposed circuit is designed to carry a load current of 10A, hence total power rating of the proposed circuit is given by

$$P_{rated} = V_{rated} * I_{rated}$$

$$P_{rated} = 254.55 * 10 = 2545.5\ watts.$$

The different types of loads the resistive and resistive-inductive (RL) loads are designed for the power rating of the circuit

The Resistive load

The load resistance = 25.45 ohm

$Load\ current = V/R$ = 254.55/25.45 = 10.001 A

$Power\ desipated\ in\ Resister$ = P = V*I = 254.55*10.001

= 2545.75 watts

The Resistive- inductive (RL) load

The RL load (choke) load - 10 A, L =64.80mH and Cos(φ) = 0.6

Hence XL= 2*π * f * L

$X_L = 2 * \pi * 50 * 64.80 * 10^{-3}$

X_L = 20.357 Ohms

The $Z = V/I$ = 254.54/10 = 25.45 $ohms$

Therefore $R = \sqrt{Z^2 - Xl^2} = \sqrt{25.45^2 - 20.35^2}$ = 15.28 $Ohms$

The Resistive – inductive load for the circuit is given by R = 15.28 Ohms and L = 64.80mH

Section 2

Modulation Technique

The control technique used to the control the switches for the proposed multilevel inverter and switching angles calculations is presented. To show the difference in THD and control technique the Equal phase control and Half Height technique angle calculations and time duration for each level is tabulated. As the Selective harmonic elimination gives the best performance with reduced THD for lower switching frequency this modulation technique is selected to implement in hardware.

Basically, the THD will depends on the modulation technique. For each level the stair case angles should be selected or calculated in such a way that it should minimize the THD because it will directly impact on the THD contribution.

Equal phase control method

The basic principle of equal phase or step control method is the time duration for all the output levels will be equal. In this method the harmonics will be higher in the output voltage wave form. This is basic fundamental modulation technique for all the multilevel inverter.

Equal phase switching angle calculations

For the quarter wave symmetry, the number of switching angle $N\alpha$ depends on the Total number of the output voltage levels.

$$N_\alpha = \frac{N_{Level} - 1}{2}$$

Where

$N\alpha$ = Number of switching angle

NL = Number of output levels

For proposed circuit number of switching angles are calculated from N_α= 30

The switching angles for each level can be calculated from the equation given by

$$\alpha_i = i * \frac{180}{2 * N_\alpha}$$

Where

i = 1,2, 3,…….30

The obtained angles were in degrees, the switching angles in the time domain can be calculated from the equation

$$t_i = \frac{\alpha_i}{360} * 0.02$$

Pulse width for each output levels is calculated by equation

Table 2: Switching angles

Output level	Angle in degrees	Angle time domain	Time period for each level
1	1.5	8.33E-05	0.000167
2	4.5	0.000250	0.000167
3	7.5	0.000417	0.000167
4	10.5	0.000583	0.000167
5	13.5	0.000750	0.000167
6	16.5	0.000917	0.000167
7	19.5	0.001083	0.000167
8	22.5	0.001250	0.000167
9	25.5	0.001417	0.000167
10	28.5	0.001583	0.000167
11	31.5	0.001750	0.000167
12	34.5	0.001917	0.000167
13	37.5	0.002083	0.000167
14	40.5	0.002250	0.000167
15	43.5	0.002417	0.000167
16	46.5	0.002583	0.000167
17	49.5	0.002750	0.000167
18	52.5	0.002917	0.000167
19	55.5	0.003083	0.000167
20	58.5	0.003250	0.000167
21	61.5	0.003417	0.000167
22	64.5	0.003583	0.000167
23	67.5	0.003750	0.000167
24	70.5	0.003917	0.000167
25	73.5	0.004083	0.000167
26	76.5	0.004250	0.000167
27	79.5	0.004417	0.000167
28	82.5	0.004583	0.000167
29	85.5	0.004750	0.000167
30	88.5	0.004917	0.000167

Table: Switching angles for equal phase technique

Half Height Method

In this method switching angles are arranged in simple manner, but the waveform at the output is not in a sine wave shape. According to the sine function a new method called Half Height Method was established new switching angles. The main switching angles are obtained from the following formula

αi =sin'1((2l-1)/(m-1))

Where

i=1,2…….(m-1)/2

The main switching angles is calculated by equation

Table 2: Switching angles

Output level	Angle in degrees	Angle time domain	Time period for each level
1	9.549739e-01	5.305410e-05	1.06E-04
2	2.865984e+00	1.592213e-04	1.06E-04
3	4.780192e+00	2.655662e-04	1.07E-04
4	6.699765e+00	3.722092e-04	1.07E-04
5	8.626927e+00	4.792737e-04	1.08E-04
6	1.056398e+01	5.868876e-04	1.08E-04
7	1.251333e+01	6.951847e-04	1.09E-04
8	1.447751e+01	8.043062e-04	1.10E-04
9	1.645925e+01	9.144028e-04	1.11E-04
10	1.846146e+01	1.025637e-03	1.13E-04
11	2.048732e+01	1.138184e-03	1.14E-04
12	2.254031e+01	1.252239e-03	1.16E-04
13	2.462432e+01	1.368018e-03	1.18E-04
14	2.674368e+01	1.485760e-03	1.20E-04
15	2.890333e+01	1.605741e-03	1.23E-04
16	3.110892e+01	1.728273e-03	1.25E-04
17	3.336701e+01	1.853723e-03	1.29E-04
18	3.568533e+01	1.982519e-03	1.33E-04
19	3.807312e+01	2.115174e-03	1.37E-04
20	4.054160e+01	2.252311e-03	1.42E-04
21	4.310467e+01	2.394704e-03	1.49E-04
22	4.577996e+01	2.543331e-03	1.56E-04
23	4.859038e+01	2.699465e-03	1.65E-04
24	5.156679e+01	2.864822e-03	1.77E-04
25	5.475249e+01	3.041805e-03	1.92E-04
26	5.821167e+01	3.233982e-03	2.13E-04
27	6.204711e+01	3.447062e-03	2.44E-04
28	6.644354e+01	3.691308e-03	2.98E-04
29	7.180513e+01	3.989174e-03	4.29E-04
30	7.952469e+01	4.418038e-03	5.82E-04

Switching angles for half height technique.

Section 3
Simulation of the Proposed Inverter

Simulation provides accurate description about the real hardware output before constructing the hardware. As a result, cost required to build the hardware prototype will be less than if we conducted the simulations by considering different test cases and for hardware the parameters are selected by considering both economical and efficiency. Simulations of cascaded Envelope type multilevel inverter with 61 level is simulated using MATLAB software. The fundamental equal phase switching pattern and Half Height technique is implemented to the circuit and simulation results were shown. The THD calculations for the simulation were obtained from the MATLAB FFT analysis window.

The proposed 61 level cascaded asymmetrical Envelope type Multilevel inverter is simulated using MATLAB/Simulink. The figure shows the circuit of the proposed MLI. The gating signals to the switches are given from pulse generators. Each level phase angle and pulse width are calculated. The IGBT switches with body diodes are used as semiconductor switching devices.

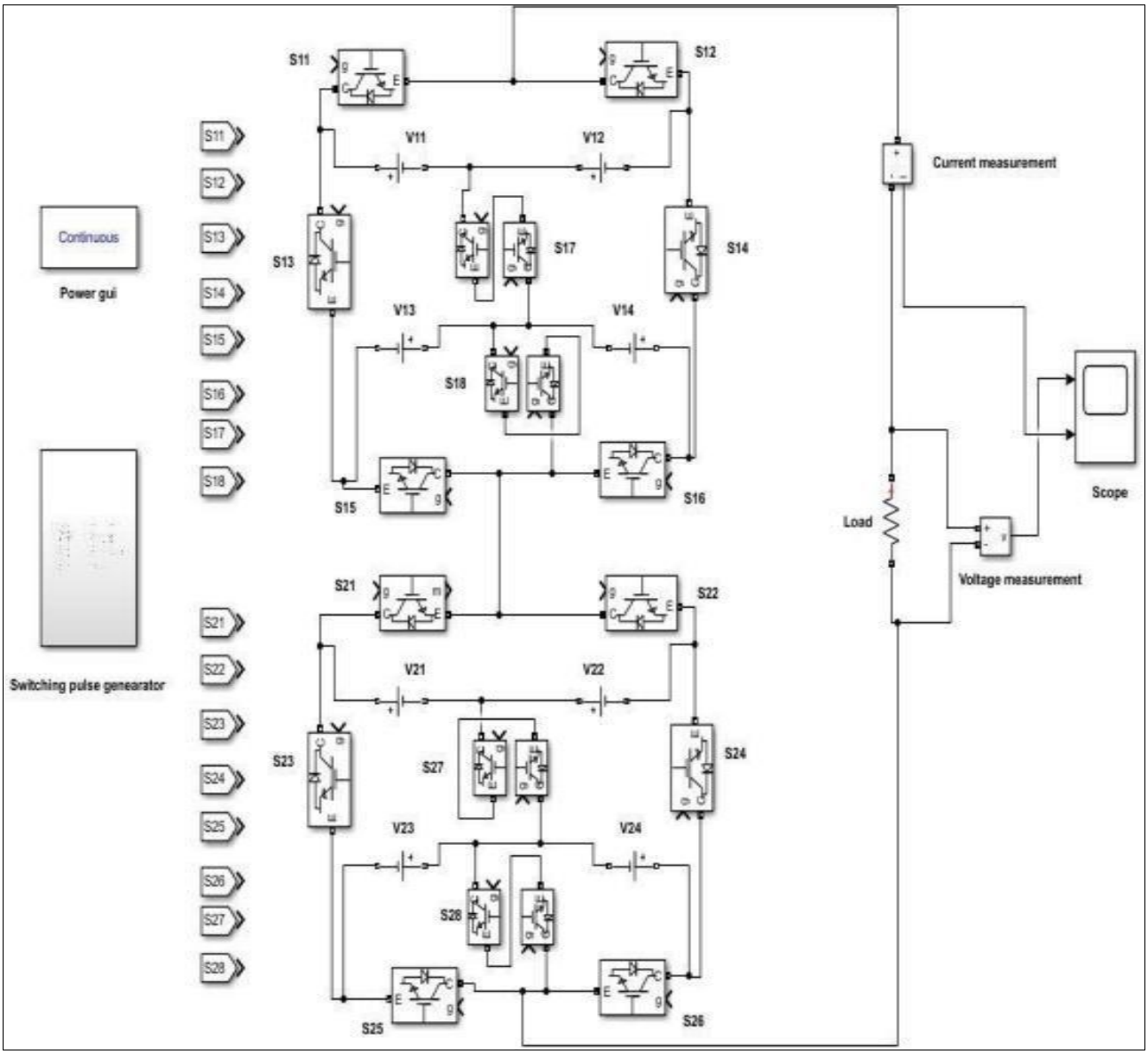


Fig 7: Simulation model of the proposed inverter

The input dc voltages are given in the binary asymmetrical pattern i.e., $V_{11} = V_{12} = 12V$, $V_{13} = V_{14} = 24V$, $V_{21} = V_{22} = 48V$, $V_{23} = V_{24} = 96V$. The Switch numbers from S11-S17 and S21=S27 are the IGBT semiconductor switches and the corresponding gating signals are shown in fig. The load connected is Resistive load Inductive load the parameters used for the simulation is given below.

Input voltages: Vdc = 12V, therefore V_1=12Vdc, V_2= 24V dc, V_3=48V dc, V_4=96V dc

Resistive load – R= 25.45ohm

Resistive – inductive (RL load), R=15.27ohm, L =64.80mH Cos(φ) = 0.6

IGBT: 600V, 10A

Internal resistance, Ron =0.001ohm

Snubber Resistance, Rs=100000ohm

Snubber capacitance, Cs= 100µF

Section 4
Simulation Results

Equal Phase Technique
Switching Pulse For 1 Full Cycle

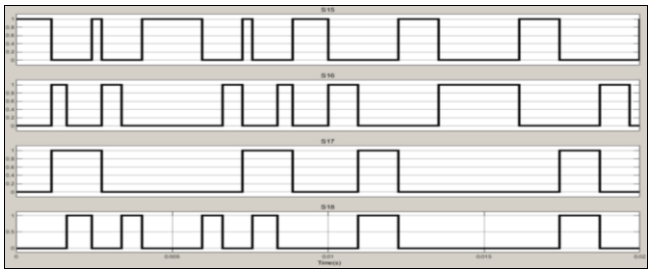


Fig 8: Gatting Signals for the switch S11 to S14

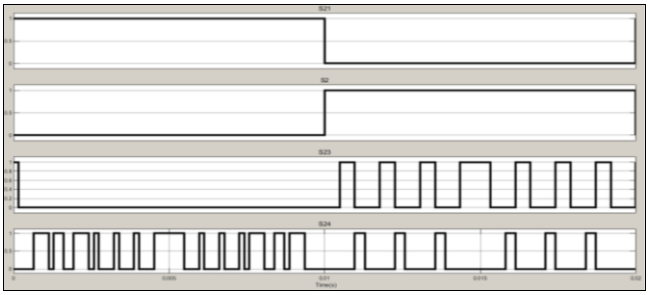


Fig 9: Gatting Signals for Switch S15 to S18

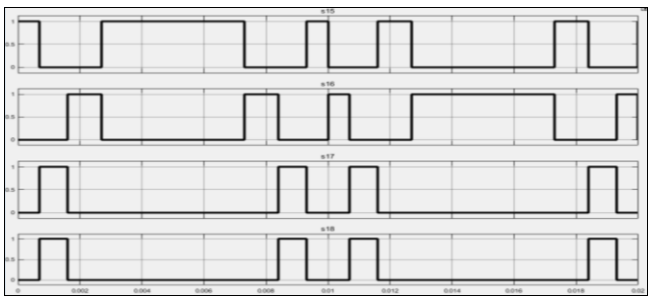


Fig 10: Getting Signals for Switch S21 to S24

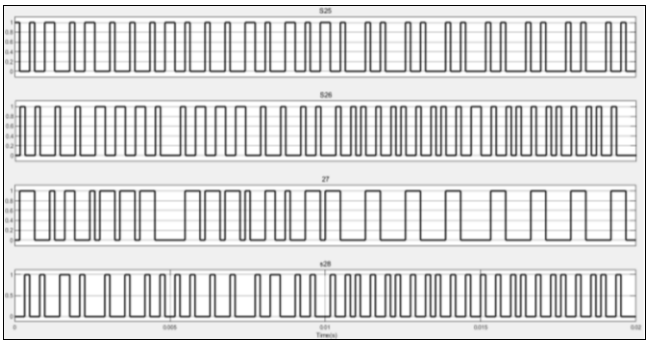


Fig 11: Getting Signals for Switch S25 to S28

Simulation results
The Fig shows the output voltage and current wave form of the proposed multilevel inverter using equal phase control method for the resistive load and resistive-inductive(RL) load. The proposed inverter has a peak voltage of 360V and R.M.S voltage of 254V. The each output voltage level is 12V. The fundamental frequency of the output voltage is 50Hz.

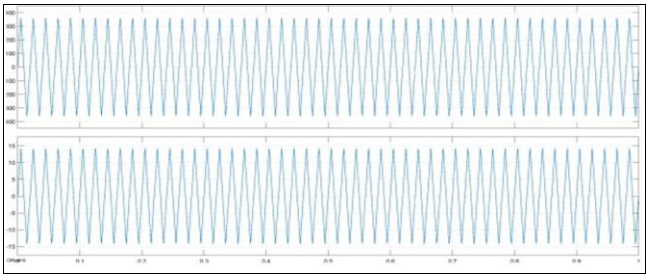


Fig 12: The output wavefrom of voltage and current for R load = 25.45ohm

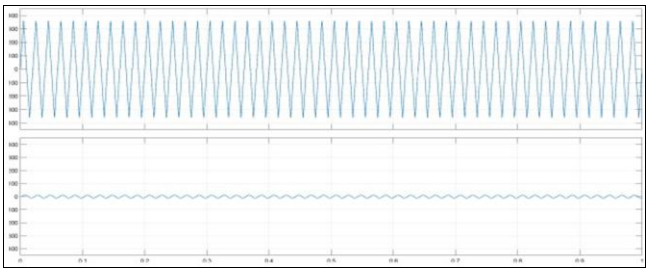


Fig 13: The output waveform of voltage and current RL load R=15.27ohm, L =64.80mH

The FFT analysis of the output waveform of voltage and current for the equal phase control method for resistive – inductive (RL) load is as shown in the Fig respectively. The obtained THD for the equal phase control method is 13.45%.and 0.13% for voltage and current waveforms.

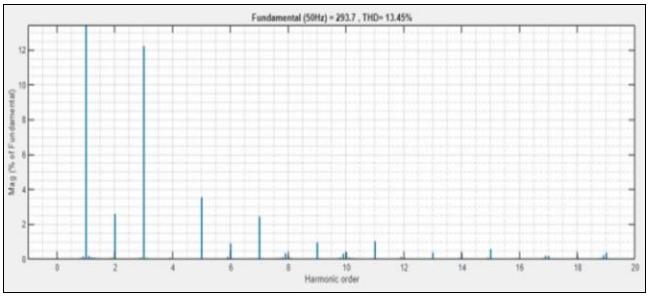


Fig 14: Total harmonic distortion of the output voltage for R load waveform

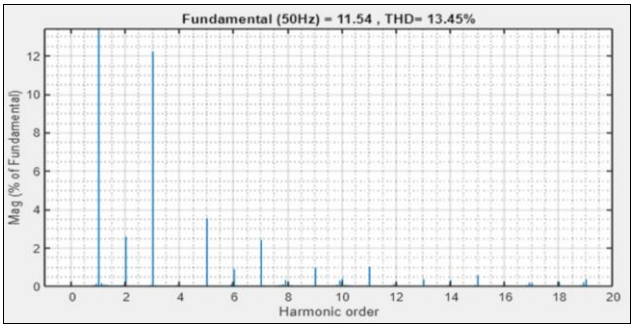


Fig 15: Total harmonic distortion of the output current for R load waveform

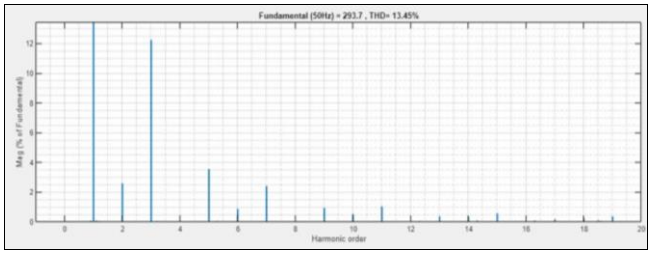


Fig 16: Total harmonic distortion of the output voltage for RL load waveform

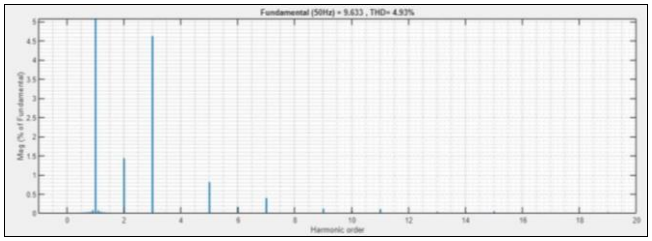


Fig 17: Total harmonic distortion of the output current for RL load waveform

Half Height Technique
Switching Pulse For 1 Full Cycle

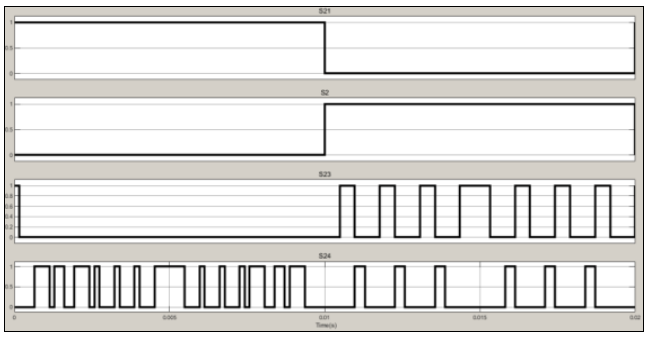


Fig 18: Gatting Signals for Switch S11 to S15

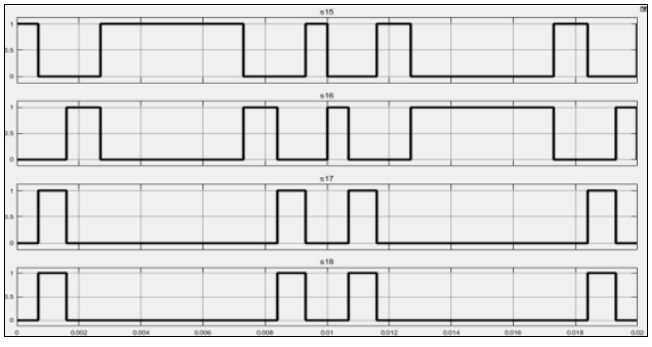


Fig 19: Gatting Signals for Switch S15 to S18

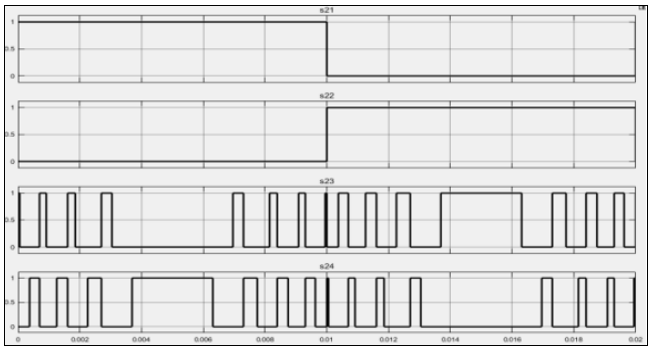


Fig 20: Gating signals for the switches S21 to S24

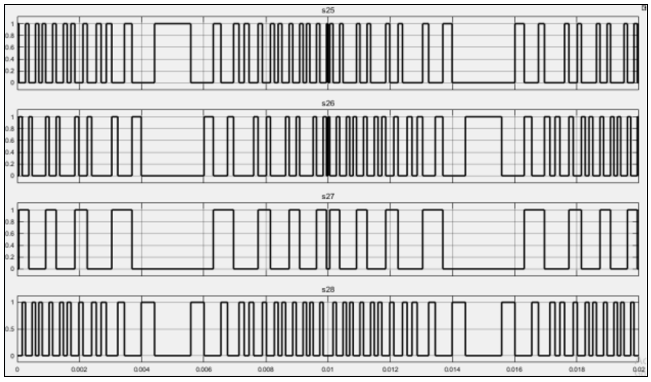


Fig 21: Gating signals for the switches S25 to S28

Simulation results

The Fig shows the output voltage and current wave form of the proposed multilevel inverter using Half Height method for the resistive load and resistive- inductive(RL) load respectively. The proposed inverter has a peak voltage of 360V and R.M.S voltage of 300V. The each output voltage level is 12V. The fundamental frequency of the output voltage is 50Hz

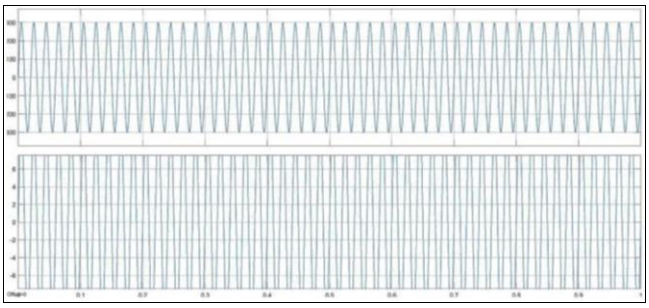


Fig 22: The output voltage and current waveform R load R= 25.45 ohm

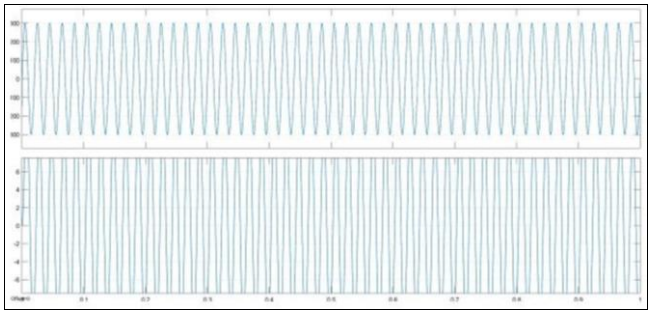


Fig 23: The output voltage and current waveform for RL load R=15.27ohm, L =64.80mH

The FFT analysis of the output wave form of voltage and current for the Selective harmonic elimination method for resistive – inductive (RL) load is as shown in the Fig respectively. The obtained THD for the Half Height method is 1.34%.and 0.13% for voltage and current wave form.

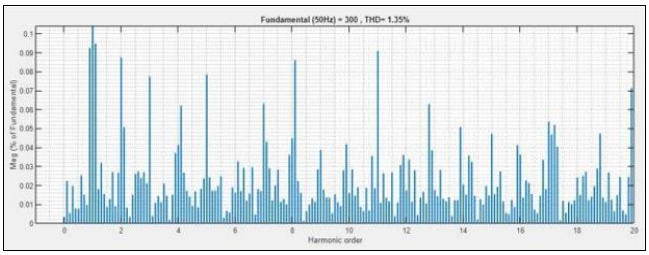


Fig 24: THD of the voltage waveform for R load using HH method

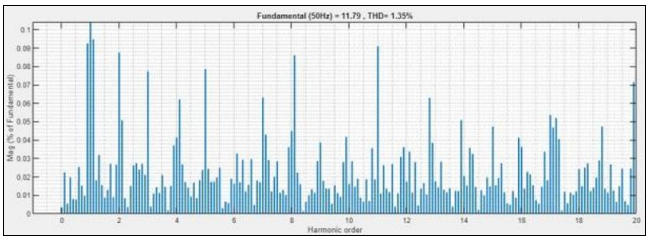


Fig 25: THD of the current waveform for R load using HH method

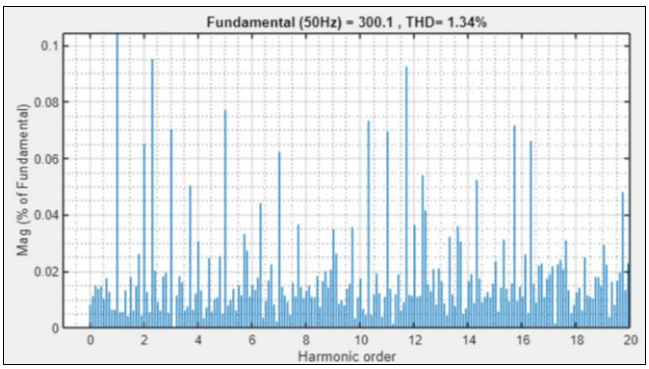


Fig 26: THD of the voltage waveform for RL load using HH method

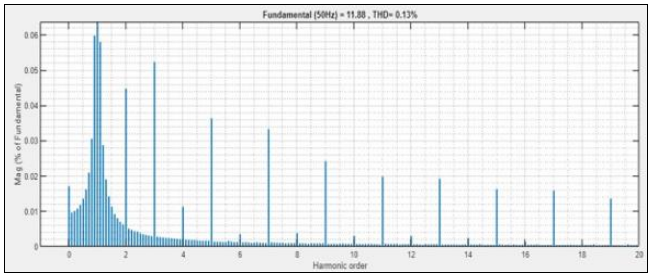


Fig 27: THD of the current waveform for RL load using HH method

3. Conclusion

The proposed 61 level Multilevel inverter us named as A new cascaded Enveloe type Asymmetrical Multilevel inverter with Binary configuration applied to DC sources, which uses 2 Envelope type modules each can individually generate 13 levels. The proposed circuit generates 61 (30 positive, 30 negative and one zero level) levels of the output waveform without using any additional H bridge circuit for the negative voltage levels. The proposed topology leads to achieve more voltage levels with different possible paths which is an advantages of the inverter in case of any failure or malfunction of a switch or driver. The proposed circuit is simulated for equal phase control method and half height method; both the methods uses the fundamental switching frequency hence it reduces the conduction losses as well. The effectiveness of the circuit is enhanced by utilizing the optimal number of the switches and DC sources which in turn decreases the cost and size of the circuit and improves the overall efficiency. The THD comparison of voltage and current output wave forms for Equal phase control method and half height method for different load condition results are established in the table.

Table 3: THD comparison of different control techniques

Envelope Type Multilevel Inverter	R load		RL load	
	Voltage	Current	Voltage	Current
Half Height method (THD)	1.34%	1.34%	1.34%	0.13%
Equal Phase Method (THD)	13.45%	13.45%	13.45%	4.93%

The THD % obtained for the proposed multilevel inverter for equal phase control and Half Height method as shown in table. The proposed multilevel inverter gives a Total harmonic distortion of 1.30% with Half height method without using any filter circuit. The MATLAB simulations results for the both control techniques and different load conditions are presented.

4. Future Scope

The proposed multilevel inverter can integrate to PV connected to grid applications and three phase system.

5. References

1. Feldman R, Tomasini M, Amankwah E, Clare JC, Wheeler PW, Trainer DR, Whitehouse RS. A Hybrid Modular Multilevel Voltage Source Converter for HVDC Power Transmission. IEEE Trans. Ind. Appl. 2013; 49(4):1577-1588.
2. Odavic M, Biagini V, Sumner M, Zanchetta P, Degano M. Low Carrier–Fundamental Frequency Ratio PWM for Multilevel Active Shunt Power Filters for Aerospace Applications. IEEE Trans. Ind. Appl. 2013; 49(1):159-167.
3. Liming Liu, Hui Li, Seon-Hwan Hwang, Jang-Mok Kim. An Energy Efficient Motor Drive with Autonomous Power Regenerative Control System Based on Cascaded Multilevel Inverters and Segmented Energy Storage. IEEE Trans. Ind. Appl. 2013; 49(1):178-188.
4. Yushan Liu, Baoming Ge, Abu-Rub H, Peng FZ. An Effective Control Method for Quasi-Z-Source Cascade Multilevel Inverter-Based Grid-Tie Single-Phase Photovoltaic Power System. IEEE Trans. Ind. Inform. 2014; 10(1):399-407.
5. Jun Mei, Bailu Xiao, Ke Shen, Tolbert LM, Jian Yong Zheng. Modular Multilevel Inverter with New Modulation Method and Its Application to Photovoltaic Grid-Connected Generator," IEEE Trans. on Power Electron. 2013; 28(11):5063-5073.
6. Rodriguez JR, Moreno-Goytia EL, Venegas-Rebollar V. A transformerless, single DC-input, DC-AC 7-levels boost converter for PV applications. North American Power Symposium (NAPS). 2011; 1(1):1-6.
7. Rodriguez J, Lai JS, Peng FZ. Multilevel inverters: A

survey of topologies, controls, and applications, IEEE Trans. on Power Electron. 2002; 49(4):724-738.
8. Nabae A, Takahashi I, Akagi H. A new neutral-point-clamped PWM inverter. IEEE Trans. Ind. Appl. IA. 1981; 17(5):518-523.
9. Meynard TA, Foch H. Multi-level choppers for high voltage applications. in Proc. Eur. Conf. Power Electron. Appl. 1992; 2:45-50.
10. Peng FZ, Lai JS, McKeever JW, Van J Coevering. Amultilevel voltage source inverter with separate DC sources for static var generation. IEEE Trans. Ind. Appl. 1996; 32(5):1130-1138.
11. Babaei E, Hosseini SH. New cascaded multilevel inverter topology with minimum number of switches, Elsevier J. Energy Convers. Manage. 2009; 50(11):2761-2767.
12. Babaei E, Kangarlu MF, Sabahi M. Extended multilevel converters: an attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters. IET Power Electron. 2014; 7(1):157-166.
13. Gupta KK, Jain S. Topology for multilevel inverters to attain maximum number of levels from given DC sources, IET Power Electron. 2012; 5(4):435-446.
14. Farhadi Kangarlu M, Babaei E. Cross-switched multilevel inverter: an innovative topology, IET Power Electronics. 2013; 6(4)642-651.
15. Ounejjar Y, Al-Haddad K, Grégoire LA. Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation. IEEE Trans. Ind. Electron. 2011; 58(4):1294-1306.